REMARKS

Claims 1-27 are pending in this application. No claims have been amended. New Claim 28 has been added. Claims 1-27 stand rejected.

Claims 1-11 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Chin et al (U.S. Pat. No. 6,202,101) in view of Kark et al (U.S. Pat. No. 6,052,772). Independent Claim 1 recites a method including receiving a first request to access data from a first memory device; preparing the first request for the data for access through the first memory device; providing a second request to access the data from a second memory device, wherein the second request is provided concurrently with the step of preparing the first request; receiving a first notification that the data associated with the first request is available from the second memory device; and terminating the first request, in response to the first notification (emphasis added).

The Office states that Chin et al. discloses this method except for terminating the first request in response to the first notification. The Applicants respectfully disagree. Chin et al. discloses a system and method for concurrently requesting I/O and memory address space while maintaining order of data sent and returned there from. The Office has pointed to multiple locations in Chin et al. where a bus interface unit dispatches multiple memory and I/O request cycles to, for example, a peripheral bus and a memory bus. However, each of these requests of Chin et al. is independent of each other and presumably request access to different data. As recited in amended Claim 1, a second request is provided to access the data from a second memory device.

The Office additionally points to Cache 16 of Fig. 1 in Chin et al. to inherently illustrate receiving a first notification (i.e., cache hit/miss) that the data associated with the first request is available from the second memory device. Applicants traverse the statement that receipt of a first notification as recited is inherent. A cache miss is an indication that data cannot be provided by the cache. A cache hit is an indication that data can be provided by cache and therefore no additional request is made. Claim 1 recites that the first notification indicates that data associated with the first request is available from the second device. Additionally, in Chin et al., after a request to a cache receives a cache miss, a second request to other memory is performed by Chin et al. In contrast, Claim 1 recites that the second request is provided concurrently with the step of preparing the first request.

Further, the Office states that Kark et al. discloses terminating the first request in response to the first notification. Kark et al. discloses a memory request protocol that allows a memory request to be withdrawn or "cancelled" without penalty so no memory resource is wasted in doing so during an assigned "cancel window." Kark et al. does not terminate requests upon receiving a first notification that the data associated with the first request is available from the second memory device as recited in Claim 1.

Because Chin et al. and Kark et al., whether taken alone or in combination, do not disclose or suggest the recited combination of elements, withdrawal of the rejection under 35 U.S.C. 103(a) is respectfully requested, and allowance of Independent Claim 1, and its dependent claims is solicited.

Claims 12-25 and 27 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Chin et al. in view of Trieu et al. (U.S. Patent No. 6,314,472).

Independent Claim 12 recites a method including receiving a first request to read data from a memory device; preparing a second request, based upon the first request, for transmission to the memory device; delivering a third request, based upon the first request, for data from a cache memory, the third request being delivered concurrently with the preparation of the second request; providing, in response to the first request, data from the cache memory when the data stored in the cache memory is coherent with the data stored in the memory device; terminating the second request when the data is provided from the cache memory; and providing, in response to the first request, data from the memory device when the data stored in the cache memory is not coherent with the data stored in the memory device (emphasis added).

The Office states that Chin et al. discloses this structure except for terminating the second request when the data is provided from the cache memory. The Applicants respectfully disagree. The Office points to the multiple locations to show multiple requests handled by Chin. However, each of these requests of Chin et al. is independent of each other and presumably request access to different data. In contrast, Claim 12 recites that a second request is based upon the first request and a third request is based on the first request.

The Office additionally states that Chin et al. implicitly teaches providing, in response to the first request, data from the cache memory when the data stored in the cache memory is coherent with the data stored in the memory device and providing, in response to the first request, data from the memory device when the data stored in the cache memory is not coherent with the data stored in the memory device. The Applicant traverses the statement of implicit teaching. In Chin et al., after a request to a cache receives a cache miss, a second request to other memory is performed by Chin et al. In contrast, Claim 12 recites that the third request being delivered concurrently with the preparation of the second request.

The Office states that Trieu et al. discloses terminating the second request when the data is provided from the cache memory. Trieu et al. discloses a computer system having a bridge that aborts read ahead accesses to system memory, responsive to disengagement of the I/O master device. In contrast to Claim 12, Trieu et al. does not terminate the second request when the data is provided from the cache memory.

Because Chin et al. and Trieu et al., whether taken alone or in combination, do not disclose or suggest the recited combination of elements, withdrawal of the rejection under 35 U.S.C. 103(a) is respectfully requested, and allowance of Independent Claim 12, and its dependent claims is solicited.

Independent Claim 19 recites a system having a data processor having: an input/output buffer; and cache memory to store data associated with a memory device; a bus interface unit having a first input/output buffer coupled to the input/output buffer of the data processor, a second input/output buffer and a third input/output buffer, said bus interface unit to: determine a validity of data in said cache memory during a cache access; and provide a notification indicating data in said cache memory is valid, wherein said notification identifies a first request; said memory device having an input/output buffer coupled, said memory device to provide data associated with a first request; a bus controller having a first input/output buffer coupled to the input/output buffer of the data processor, a second input/output buffer coupled to the second input/output buffer of the bus interface unit and a third input/output buffer, said bus controller to: receive said first request to access data in said memory device, wherein said request is received from a bus client; provide said first request to the memory controller; receive said data associated with said first request from said bus interface unit; the memory controller having a first input/output buffer coupled to the third input/output buffer of the bus controller, a second input/output buffer coupled to the third input/output buffer of the bus interface unit and a third input/output buffer coupled to the input/output buffer of the memory device, said memory controller to: provide access to said memory device; receive said first request from said bus controller; prepare said first request to access data from said memory device; provide a second request to said bus interface unit, wherein said second request is to access data associated with said first request from said cache memory; receive said notification from said bus interface unit; and terminate the first request, in response to the receipt of said notification (emphasis added).

The Office states that Chin et al. discloses this structure except for terminating the first request in response to the receipt of said notification. The Applicants respectfully disagree. The Office states that Chin et al. implicitly teaches said notification identifies a first request because when the CPU or I/O device generates a plurality of requests, each request must have its own identification so the memory controller can return requested data to appropriate request. The Applicant traverses the statement of implicit teaching. Claim 19 recites that said first request is to access data in said memory device and said second request is to access data from the cache memory. Therefore, as recited in Claim 19, the notification is associated to the second request, but identifies the first request, whereas in Chin et al., the request identifies itself.

The Office states that Trieu et al. discloses terminating the first request in response to the receipt of said notification. Trieu et al. discloses a computer system having a bridge that aborts read ahead accesses to system memory, responsive to disengagement of the I/O master device. Trieu et al. does not terminate a request upon receiving a notification indicating data in cache memory is valid as recited in Claim 19.

Because Chin et al. and Trieu et al., whether taken alone or in combination, do not disclose or suggest the recited combination of elements, withdrawal of the rejection under 35 U.S.C. 103(a) is respectfully requested, and allowance of Independent Claim 19, and its dependent claims is solicited.

Claim 26 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Chin et al., Trieu et al. and further in view of Nakano et al. (U.S. Patent No. 6,263,406). Claim 26 depends from allowable Claim 19 (allowable as illustrated above) and is allowable for at least this reason.

New Claim 28 recites a cache memory; a memory device; and a memory controller configured to: provide access to said memory device; receive a first request to access data in said memory device; prepare said first request to access data from said memory device; provide a second request to access data associated with said first request from said cache memory; receive a notification indicating data in said cache memory is valid, wherein said notification identifies the first request; and terminate the first request, in response to the receipt of said notification (emphasis added).

As illustrated above, Chin et al. and Trieu et al, and the other cited references, do not teach or suggest providing a second request to access data from cache memory, receiving a notification indicating data in cache memory is valid, wherein said notification identifies the first request and terminating the first request in response to the receipt of the notification.

Because the cited references, including Chin et al. and Trieu et al., whether taken alone or in combination, do not disclose or suggest the recited combination of elements, withdrawal of the rejection under 35 U.S.C. 103(a) is respectfully requested, and allowance of Independent Claim 28 is solicited.

Based on the remarks herein, it is believed that each pending independent claim is in condition for allowance. In addition, the dependent claims provide additional points of novelty. Any assertions of inherency made by the Office are hereby respectfully traversed.

In conclusion, Applicant(s) has overcome all of the Office's rejections, and early notice of allowance to this effect is earnestly solicited. If, for any reason, the Office is unable to allow the Application on the next Office Action, and believes a telephone interview would be helpful, the Examiner is respectfully requested to contact the undersigned attorney.

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to the Commissioner for Patents on 7-11-03.

Katrina Prati
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